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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,153	01/20/2004	Xiaopeng Chen	MP0417	4951

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EXAMINER	
PHU, SANH D	
ART UNIT	PAPER NUMBER
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/762,153	CHEN ET AL.	
	Examiner	Art Unit	
	Sanh D. Phu	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4 and 11-23, 30-34, 41-45 and 52-58 are rejected under 35 U.S.C. 102(e) as being anticipated by Tellado et al (2005/0088961).

-Regarding to claim 1, see figures 3 and 7, and [0029-0033, 0050-0058, 0071-0086], Tellado et al discloses a transceiver (315a, 325a) (see figure 3) comprising:

a receiver (325a) (see figure 3) to receive an analog communication signal (R1A), the analog communication signal containing an interference signal;

a digital compensation circuit (comprising (730, 740) (see figure 7)) to generate a digital replica of the interference signal contained in the analog communication signal;

a converter (735) (see figure 7) to convert the digital replica of the interference signal into a corresponding analog replica of the interference signal; and

a subtraction circuit (SUM) (see figure 7) to subtract the analog replica of the interference signal from the analog communication signal (R1A).

-Regarding to claim 2, Tellado et al discloses that the digital compensation circuit includes an echo canceller (740) (see figure 7)to generate a digital replica of an echo interference signal in the analog communication signal (see [0054]).

-Regarding to claim 3, Tellado et al discloses that the digital compensation circuit further includes a near-end crosstalk (NEXT) canceller (730) (see figure 7)to generate a digital replica of a NEXT interference signal in the analog communication signal (see [0053]).

-Regarding to claim 4, Tellado et al discloses an analog-to-digital converter (ADC)(790)(see figure 7) to sample the analog communication signal having the analog replica subtracted therefrom, and generate a digital signal that is substantially devoid of the interference signal (see [0057-0058]).

-Regarding to claim 11, Tellado et al discloses that the transceiver is a 1000Base-TX complaint (considered here equivalent with the limitation "IEEE 1000Base-TX complaint") (see [0003]).

-Regarding to claim 12, as similarly applied to claims 1-4 and 11 set forth above and herein incorporated, Tellado et al discloses a method for reducing interference signals in an analog communication signal, the method comprising:

procedure (325) (see figure 3) of receiving an analog communication signal (R1A) through a receiver (325), the analog communication signal containing an interference signal;

procedure (comprising (730, 740) (see figure 7)) of generating a digital replica of the interference signal contained in the analog communication signal;

procedure (735) (see figure 7)converting the digital replica of the interference signal into a corresponding analog replica of the interference signal; and

procedure (SUM) (see figure 7) of subtracting the analog replica of the interference signal from the analog communication signal to substantially cancel the interference signal from the analog communication signal.

-Claim 13 is rejected with similar reasons set forth for claim 2.

-Claim 14 is rejected with similar reasons set forth for claim 3.

-Regarding to claim 15, Tellado et al discloses that generating a digital replica of the interference signal includes:

procedure of determining cancellation coefficients "est_ha" that model an impulse response of the interference signal (see [0072-0086]); and

procedure of multiplying the cancellation coefficients with a communication signal from a transmitter that causes the interference signal (see [0081]).

-Regarding to claim 16, Tellado et al discloses that determining cancellation coefficients includes determining cancellation coefficients using an adaptive filter (see [0078-0086]).

-Claim 17 is rejected with similar reasons set forth for claim 4.

-Regarding to claim 18, Tellado et al discloses that generating a digital replica of the interference signal includes generating a digital replica of a portion (NEXT or ECHO) of the interference signal (see figure 7).

-Regarding to claim 19, in Tellado et al, the portion of the interference signal, as a signal, inherently has a voltage level(s), (the portion considered here equivalent with the limitation "high voltage portions").

-Regarding to claim 20, as similarly applied to claims 1-4 and 11-19 set forth above and herein incorporated, Tellado et al discloses a transceiver comprising:

receiving means (325) (see figure 3) for receiving an analog communication signal (R1A), the analog communication signal containing an interference signal;

generating means (comprising (730, 740) (see figure 7))for generating a

digital replica of the interference signal contained in the analog communication signal;

converting means (735) (see figure 7) for converting the digital replica of the interference signal into a corresponding analog replica of the interference signal; and

subtracting means (SUM) (see figure 7) for subtracting the analog replica of the interference signal from the analog communication signal to substantially cancel the interference signal from the analog communication signal (R1A).

-Claim 21 is rejected with similar reasons set forth for claim 2.

-Claim 22 is rejected with similar reasons set forth for claim 3.

-Claim 23 is rejected with similar reasons set forth for claim 4.

-Claim 30 is rejected with similar reasons set forth for claim 11.

-Regarding to claim 31, as similarly applied to claims 1-4 and 11-23, 30 set forth above and herein incorporated, Tellado et al discloses a network device in a communication system, the network device (see figure 3) comprising a transceiver (315a, 325a) (see figure 3) operable to receive an

analog communication signal (R1A)containing an interference signal, the transceiver including:

a receiver (325) (see figure 3) to receive the analog communication signal;

a digital compensation circuit (comprising (730, 740) (see figure 7)) to generate a digital replica of the interference signal contained in the analog communication signal;

a converter (735) (see figure 7) to convert the digital replica of the interference signal into a corresponding analog replica of the interference signal; and

a subtraction circuit (SUM) (see figure 7) to subtract the analog replica of the interference signal from the analog communication signal.

-Claim 32 is rejected with similar reasons set forth for claim 2.

-Claim 33 is rejected with similar reasons set forth for claim 3.

-Claim 34 is rejected with similar reasons set forth for claim 4.

-Claim 41 is rejected with similar reasons set forth for claim 11.

-Regarding to claim 42, as similarly applied to claims 1-4 and 11-23, 30-34, 41 set forth above and herein incorporated, Tellado et al discloses a

network device in a communication system, the network device comprising communication means (315a, 325a) (see figure 3) for receiving an analog communication signal (R1A) containing an interference signal, the communication means including:

receiving means (325a) (see figure 3)for receiving the analog communication signal;

generating means (comprising (730, 740) (see figure 7)) for generating a digital replica of the interference signal contained in the analog communication signal;

converting means (735) (see figure 7) for converting the digital replica of the interference signal into a corresponding analog replica of the interference signal; and

subtracting means (SUM) (see figure 7) for subtracting the analog replica of the interference signal from the analog communication signal to substantially cancel the interference signal from the analog communication signal.

-Claim 43 is rejected with similar reasons set forth for claim 2.

-Claim 44 is rejected with similar reasons set forth for claim 3.

-Claim 45 is rejected with similar reasons set forth for claim 4.

-Claim 52 is rejected with similar reasons set forth for claim 11.

-Regarding to claim 53, as similarly applied to claims 1-4 and 11-23, 30-34, 41 set forth above and herein incorporated, Tellado et al discloses a cancellation system (see figure 3) for use in a communication system including a communication line (312), the communication line having a transmitter (e.g., (315a)) and a receiver (e.g., (325a)) at each end, the cancellation system to reduce interference signals in an analog communication signal (R1A) received by a receiver (525a), the cancellation system comprising:

an echo canceller (comprising (740) (see figure 7)) associated with a receiver, the echo canceller_ to receive a transmitted signal (S1A', S2A', S3A', S4A')from a transmitter in a same transceiver as the receiver with which the echo canceller is associated, the echo canceller operable to generate a digital replica echo interference signal based on the transmitted signal;

a converter (735) (see figure 7) to convert the digital replica of the echo interference signal into a corresponding analog replica of the echo interference signal; and

a subtracter (SUM) (see figure 7) to subtract the replica echo interference signal from an analog communication signal received by the receiver.

-Regarding to claim 54, as similarly applied to claims 1-4 and 11-23, 30-34, 41-45, 52, 53, set forth above and herein incorporated, Tellado et al discloses a cancellation system for use in a communication system (see figure 3) including a communication line (312), the communication line having a transmitter and a receiver at each end, the cancellation system to reduce interference signals in an analog communication signal received by a receiver, the cancellation system comprising:

a NEXT canceller (730) (see figure 7)associated with a receiver, the NEXT canceller to receive a transmitted signal (S1A', S2A', S3A', S4A') from a local transmitter, the NEXT canceller operable to generate a digital replica NEXT interference signal based on the transmitted signal;

a converter (735) (see figure 7) to convert the digital replica of the NEXT interference signal into a corresponding analog replica of the NEXT interference signal; and

a subtracter (SUM) (see figure 7) to subtract the replica NEXT interference signal from an analog communication signal received by the receiver.

-Regarding to claim 55, as similarly applied to claims 1-4 and 11-23, 30-34, 41-45, 52, 53, 54, set forth above and herein incorporated, Tellado et al discloses a cancellation system for use in a communication system (see figure 3) including a communication line (312), the communication line having a transmitter and a receiver at each end, the cancellation system to reduce interference signals in an analog communication signal (R1A) received by a receiver (325a), the cancellation system comprising:

echo cancellation means (740) (see figure 7) associated with a receiver, the echo cancellation means to receive a transmitted signal (S1A', S2A', S3A', S4A') from a transmitter in a same transceiver as the receiver with which the echo cancellation means is associated, the echo cancellation means for

generating a digital replica echo interference signal based on the transmitted signal;

converting means (735) (see figure 7) for converting the digital replica of the echo interference signal into a corresponding analog replica of the echo interference signal; and

subtracting means (SUM) (see figure 7) for subtracting the replica echo interference signal from an analog communication signal (R1A) received by the receiver.

-Regarding to claim 56, as similarly applied to claims 1-4 and 11-23, 30-34, 41-45, 52-55, set forth above and herein incorporated, Tellado et al disclose a cancellation system for use in a communication system (see figure 3) including a communication line (312), the communication line having a transmitter and a receiver at each end, the cancellation system to reduce interference signals in an analog communication signal received by a receiver, the cancellation system comprising:

NEXT cancellation means (730) (see figure 7) associated with a receiver, the NEXT cancellation means to receive a transmitted signal from

a local transmitter, the NEXT cancellation means for generating a digital replica NEXT interference signal based on the transmitted signal;

converting means (735) (see figure 7) for converting the digital replica of the NEXT interference signal into a corresponding analog replica of the NEXT interference signal; and

subtracting means (SUM) (see figure 7) for subtracting the replica NEXT interference signal from an analog communication signal received by the receiver.

-Regarding to claim 57, as similarly applied to claims 1-4 and 11-23, 30-34, 41-45, 52-56, set forth above and herein incorporated, Tellado et al disclose a method (see figure 3) for reducing interference signals in an analog communication signal (R1A) received by a receiver (325A) of a communication line (312), the method comprising:

procedure (710, 720) (see figure 7) of receiving a transmitted signal (S1A', S2A', S3A', S4A') from a transmitter in a same transceiver as a receiver;

procedure (740)(see figure 7) of generating a digital replica echo interference signal based on the transmitted signal;

procedure (735) (see figure 7) of converting the digital replica of the echo interference signal into a corresponding analog replica of the echo interference signal; and

procedure (SUM) (see figure 7) of subtracting the replica echo interference signal from an analog communication signal received by the receiver.

-Regarding to claim 58, as similarly applied to claims 1-4 and 11-23, 30-34, 41-45, 52-57, set forth above and herein incorporated, Tellado et al disclose a method for reducing interference signals in an analog communication signal (R1A) (see figure 3) received by a receiver (325A)of a communication line (312), the method comprising:

procedure ((710, 720) (see figure 7) of receiving a transmitted signal (S1A', S2A', S3A', S4A') from a transmitter local to a receiver;

procedure (730) (see figure 7) of generating a digital replica NEXT interference signal based on the transmitted signal;

procedure (735) (see figure 7) converting the digital replica of the NEXT interference signal into a corresponding analog replica of the NEXT interference signal; and

procedure (SUM) (see figure 7) subtracting the replica NEXT interference signal from an analog communication signal received by the receiver.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5, 24, 35, 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tellado et al in view of Druihe (6,452,967).

-Regarding to claims 5, and similarly applied to claims 24, 35, 46, Tellado et al does not teach a FIFO buffer to receive the digital signal and store the digital signal on a first-in-first-out basis.

Druihe teaches a phase locked loop (PLL) for providing a clock signal (CLK) for an ADC (A/D CONVERTER) and a FIFO buffer (MM) to receive the digital signal and store and retrieve the digital signal output of the ADC on a first-in-first-out basis in order to absorb the jitter of the phase locked loop (see figure 2, and col. 8, lines 56-63).

Since in Tellado et al, a clock signal is inherently needed in the ADC for sampling the analog communication signal, and Tellado et al does not teach how the clock signal of the ADC is provided, it would have been obvious for a person skilled in the art to additionally implement Tellado et al with a phase locked loop and a FIFO buffer, as taught by Druihe, in such a way that the phase locked loop would provide the clock signal for the ADC, and the FIFO would receive and retrieve the digital signal on a first-in-first-out basis for further processing so that with such the implementation, the clock signal would be provided as required and the digital signal of the ADC outputted from the FIFO buffer would be free of jitter and ready for further processing.

5. Claims 6-10, 25-29, 36-40, 47-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tellado et al in view of Druihe and further in view of Roo (6,775,529).

-Regarding to claim 6, and similarly applied to claims 25, 36, 47, Tellado et al in view of Druihe does not teach a feed forward equalizer (FFE) to receive the digital signals from the FIFO buffer, the FFE operable to filter individual digital signals, as claimed.

Roo teaches using a FFE (16) to remove intersymbol interference from a received digital signal (see figure 4, col. 6, lines 15-19).

It would have been obvious for a person skilled in the art to additionally implement Tellado et al invention in view of Druihe with a FFE, as taught by Roo, in such a way that the FFE would filter individual digital signals in order to remove possible intersymbol interference from the digital signals outputted from the FIFO buffer so that the digital signals would be free of possible intersymbol interference for further processing.

-Regarding to claim 7, and similarly applied to claims 26, 37, 48, Tellado et al in view of Druihe and Roo does not teach that the FFE is LMS type adaptive

filter. However, Tellado et al in view of Druihe and Roo teach that the FFE is a finite impulse response (FIR) equalizer (see Roo, col. 5, lines 2-7). On the other hand, implementing a FIR equalizer as a LMS type adaptive filter is well-known in the art, and the examiner takes Official Notice. Since Tellado et al in view of Druihe and Roo does not teach in detail how the FFE is implemented, it would have been obvious for a person skilled in the art to implement the FFE as a LMS type adaptive filter so that the FFE would be provided as required.

-Regarding to claim 8, and similarly applied to claims 27, 38, 49, Tellado et al in view of Druihe and Roo teaches that the invention is configurable to further comprise a data detector to detect data from the filtered individual digital signals (see Roo, (18) of figure 4).

-Regarding to claim 9, and similarly applied to claims 28, 39, 50, Tellado et al in view of Druihe and Roo teaches that the data detector is a Viterbi detector detector to detect data from the filtered individual digital signals.

-Regarding to claim 10, and similarly applied to claims 29, 40, 51, in Tellado et al in view of Druihe and Roo, inherently the data is an electrical data symbol (see Roo, (PSC) of figure 4).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sanh D. Phu whose telephone number is (571)272-7857. The examiner can normally be reached on M-Th from 7:00-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew D. Anderson can be reached on (571) 272-4177. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sanh D. Phu
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SP

2/8/07

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